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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,390	HA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,33 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,33 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-16, 33 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase “as if the code symbols constitute a perfect 2m * J matrix” is indefinite since “as if” suggests a hypothetical that never occurs and hence cannot have a real tangible connection to the method. The Examiner assumes the Applicant intended --independently of the remainder values--.

Response to Arguments

Applicant's arguments filed 05/14/2009 have been fully considered but they are not persuasive.

The Applicant contends, “Even if the Examiner's interpretation is correct, in no way does such a disclosure teach any feature in as complete detail as claimed in claim 1. Specifically, the alleged code symbols in TIA/E1A/IS-2000.2-A-I are not written in a 2^m * J matrix where R is the number of remaining bits in the last column J. As stated by the Examiner, R in TIA/EIA/IS- 2000.2-A-1 is the number of bits exceeding the first 2^{n-1}

columns. Therefore, in an array of 2^n columns, R must partially fill 2^{n-1} columns. Clearly, this teaching cannot be equated with the claimed feature discussed above".

The Examiner disagrees and asserts that lines 8-11 of page 2-110 and Footnote 12 and page 2-111 in TIA/EIA/IS-2000.2-A-1 clearly teaches that the address generation is equivalent to writing turbo coded input bits to a $2^{n-1} * 2^5$ matrix at specific addresses specified by the input counter values to the Address calculator of Figure 2.1.3.1.4.2.3-1 on page 2-111 whereby the 5 LSBs $i_4 \ldots i_0$ represent row addresses and the n MSBs represent $i_{n+4} \ldots i_5$ column addresses and whereby the output of the Address calculator of Figure 2.1.3.1.4.2.3-1 on page 2-111 represents the a read address form the $2^{n-1} * 2^5$ matrix. Step 1 in lines 5-7 on page 2-111 of TIA/EIA/IS-2000.2-A-1 teaches that a number of N_{turbo} bits whereby whereby $2^{n+4} \leq N_{turbo} \leq 2^{n+5}$ are substantially mapped to the $2^5 x 2^n$ element matrix. Note: TIA/EIA/IS-2000.2-A-1 clearly suggests that N_{turbo} does not need to equal to 2^{n+5} an can be less than 2^{n+5}, but greater than $2^{(n-1)+5}$, that is, $N_{turbo} = 2^{(n-1)+5} + R$ whereby R represents the number of bits exceeding $2^{(n-1)+5}$; clearly setting m = n-1 and $J=2^5$ so that $2^{(n-1)+5} = 2^{n-1} * 2^5 = 2^m * J$ and rewriting the equation representing the number N_{turbo} of bits as $N_{turbo} = 2^m * J + R$ does not require any modification to or constitute any change to the algorithm on pages 2-110 to 2-112 of TIA/EIA/IS-2000.2-A-1. The Examiner asserts "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, **but this is not an ipsissimis verbis test, i.e., identity of terminology is not required**. In re Bond, 910 F.2d 831, 15 USPQ2d

1566 (Fed. Cir. 1990). Hence rewriting $N_{turbo} = 2^{(n-1)+5} + R$ in the form $N_{turbo} = 2^m * J + R$ does not constitute a patentable distinction from TIA/EIA/IS-2000.2-A-1.

The Applicant contends that "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol as if the code symbols constitute a perfect 2m * J matrix" in TIA/EIA/IS-2000.2-A-1 is not the same as in the Applicants' claim 1.

The Examiner disagrees and asserts lines 8-11 of page 2-110 and Footnote 12 and page 2-111 in TIA/EIA/IS-2000.2-A-1 clearly teaches that the address generation is equivalent to writing turbo coded input bits to a $2^{n-1} * 2^5$ matrix at specific addresses specified by the input counter values to the Address calculator of Figure 2.1.3.1.4.2.3-1 on page 2-111 whereby the 5 LSBs $i_4 \ldots i_0$ represent row addresses and the n MSBs represent $i_{n+4} \ldots i_5$ column addresses and whereby the output of the Address calculator of Figure 2.1.3.1.4.2.3-1 on page 2-111 represents the a read address form the $2^{n-1} * 2^5$ matrix. Figure 2.1.3.1.4.2.3-1 on page 2-111 in TIA/EIA/IS-2000.2-A-1 teaches that the row addresses $i_4 \ldots i_0$ are bit reversed to produce interim address $i_0 \ldots i_4$ and interim address $i_0 \ldots i_4$ is appended to address compensation factor $t_{n-1} \ldots t_0$ to generate a output read address. TIA/EIA/IS-2000.2-A-1 specifically teaches generating an interim address by bit reversal order (BRO) operation on an index of a code symbol as if the code symbols constitute a perfect 2m * J matrix (Bit reverse in Figure 2.1.3.1.4.2.3-1 on page 2-111 of TIA/EIA/IS-2000.2-A-1 is performed on the 5 LSBs independently of what R is and for all practical purposes R, that is, Bit reverse in Figure 2.1.3.1.4.2.3-1 and in

step 6 on page 2-111 of TIA/EIA/IS-2000.2-A-1 is performed exactly the same way for any value R on each LSB address position $i_0 \ldots i_4$ as if the remainder R is 0 and as if the code symbols constitute a perfect $2^m * J$ matrix independent of the remainder R; $i_0 \ldots i_4$ in Figure 2.1.3.1.4.2.3-1 is an interim address; Note: Bit reverse is performed on row addresses $i_4 \ldots i_0$ independantly of the number of columns in the matrix and independently of whether there exits R remainder values)

The Applicant contends that "calculating an address compensation factor for compensating the interim address based on the number of the R code symbols written in the last column J" in TIA/EIA/IS-2000.2-A-1 is not the same as in the Applicants' claim 1.

The Examiner disagrees and asserts that column addresses $i_{n+4} \ldots i_5$ correspond to columns of the $N_{turbo} = 2^m * J + R = 2^5 2^{n-1} + R$ bits in the $2^5 x 2^n$ element matrix of TIA/EIA/IS-2000.2-A-1. Figure 2.1.3.1.4.2.3-1 on page 2-111 in TIA/EIA/IS-2000.2-A-1 teaches that that column addresses $i_{n+4} \ldots i_5$ corresponding to all columns in the $2^5 x 2^n$ element matrix including the number of R code symbols written to the last column. Clearly TIA/EIA/IS-2000.2-A-1 teaches a step for generating an address compensation factor $t_{n-1} \ldots t_0$ for compensating the interim address $i_0 \ldots i_4$ based on the number of the R code symbols written in the last column J since the address compensation factor $t_{n-1} \ldots t_0$ is based on column addresses $i_{n+4} \ldots i_5$ corresponding to all columns in the $2^5 x 2^n$ element matrix including the number of R code symbols written to the last column.

The Applicant contends that "generating a read address by adding the interim address and the address compensation factor for the code symbol" in TIA/EIA/IS-2000.2-A-1 is not the same as in the Applicants' claim 1.

The Examiner disagrees and asserts Figure 2.1.3.1.4.2.3-1 on page 2-111 in TIA/EIA/IS-2000.2-A-1 that the address compensation factor $t_{n-1}\ldots t_0$ is added to the interim address $i_0\ldots i_4$ sequence to generate an output address. Note: The Authoritative Dictionary of IEEE Standards Terms defined "add" as "to insert a record into an existing file" and Merriam-Webster's dictionary defines "add" as "to include as member of a group".

The Applicant contends, "Applicants believe that the Examiner clearly does not fully comprehend the scope of the present application and its relation to the cited art".

The Examiner would like to point out that the current rejections are based on the language in the claims and its relation to the cited art, not the "the scope of the present application" and its relation to the cited art. It is the Examiner's position that the current claim language that the Applicant uses to claim the Applicant's invention reads on the Prior Art. Specifically, claim 5 of U. S. Patent No. US 6668350 B1 is directed to generating read addresses from write addresses used to write input data to a $2^m * J$ matrix. Reciting in the Applicant's claim 1 of the current application that the matrix is a $2^m * J$ matrix with an additional column of R bits does not distinguish from the prior art since any $2^m * J$ matrix can be designated as $2^m * J'$ matrix with an additional column of R bits where J' = J-1 and R is equal to the number of bits in the last column of the

original 2^m * J matrix. Changing the way a matrix is described does not change the matrix. "The identical invention must be shown in as complete detail **as is contained in the ... claim**" [Emphasis added]. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, **but this is not an ipsissimis verbis test, i.e., identity of terminology is not required**. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The Applicant contends, "The read address cited by Kim for reading code symbols, however, does not include any compensation for a remaining number of bits R formed in the last column that does not complete the last column".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "compensation for a remaining number of bits R formed in the last column that does not complete the last column") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Nowhere does claim 1 recite or suggest, "compensation for a remaining number of bits R formed in the last column that does not complete the last column". Claim 1 simply states, "calculating an address compensation factor for compensating the interim address based on the number of the R code symbols written in the last column J".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over TIA/EIA/IS-2000.2-A-1 (TIA/EIA/IS-2000.2-A-1, "Physical Layer Standard for CDMA2000 Spread Spectrum Systems", TELECOMMUNICATIONS INDUSTRY ASSOCIATION, November 2000) in view of Tiedemann, Jr.; Edward G. et al. (US 6351460 B1, hereafter referred to as Tiedemann).

35 U.S.C. 103(a) rejection of claim 1.

TIA/EIA/IS-2000.2-A-1 teaches A method for reading code symbols by deinterleaving to decode an encoder packet in a receiver for a mobile communication system supporting interleaving, wherein an interleaved encoder packet has (2^m * J +R) bits wherein the

symbol codes code symbols are written in the format of a 2^m * J matrix and R is the number of remaining bits in the last column J (lines 8-11 on page 2-110 and footnote 12 on page 2-111 of TIA/EIA/IS-2000.2-A-1 teaches that the address generator of Figure 2.1.3.1.4.2.3-1 on page 2-111 is substantially an address generator for a packet having 2^5x2^n elements; Step 1 in lines 5-7 on page 2-111 of TIA/EIA/IS-2000.2-A-1 teaches that a number of N_{turbo} bits whereby whereby $2^{n+4} \leq N_{turbo} \leq 2^{n+5}$ are substantially mapped to the 2^5x2^n element matrix; Note: TIA/EIA/IS-2000.2-A-1 clearly suggests that N_{turbo} does not need to equal to 2^{n+5} an can be less than 2^{n+5}, but greater than $2^{(n-1)+5}$, that is, $N_{turbo} = 2^{(n-1)+5} + R$ whereby R represents the number of bits exceeding $2^{(n-1)+5}$; clearly setting m = n-1 and $J=2^5$ so that $2^{(n-1)+5} = 2^{n-1} * 2^5 = 2^m * J$ and rewriting the equation representing the number N_{turbo} of bits as $N_{turbo} = 2^m * J + R$ does not require any modification to or constitute any change to the algorithm on pages 2-110 to 2-112 of TIA/EIA/IS-2000.2-A-1), the method comprising the steps of: generating an interim address by bit reversal order (BRO) operation on an index of a code symbol as if the code symbols constitute a perfect 2m * J matrix (Bit reverse in Figure 2.1.3.1.4.2.3-1 on page 2-111 of TIA/EIA/IS-2000.2-A-1 is performed on the 5 LSBs independently of what R is and for all practical purposes R, that is, Bit reverse in Figure 2.1.3.1.4.2.3-1 and in step 6 on page 2-111 of TIA/EIA/IS-2000.2-A-1 is performed exactly the same way for any value R on each LSB address position $i_0 \ldots i_4$ as if the remainder R is 0 and as if the code symbols constitute a perfect 2^m * J matrix independent of the remainder R; $i_0 \ldots i_4$ in Figure 2.1.3.1.4.2.3-1 is an interim address); calculating an address compensation factor for compensating the interim address based on the number of the R code

symbols written in the last column J (the Multiply and Select block of Figure 2.1.3.1.4.2.3-1 and in step 5 on page 2-111 of TIA/EIA/IS-2000.2-A-1 is a step for an address compensation factor $t_{n-1}\ldots t_0$ based on the remaining bits including the R remaining of the $N_{turbo} = 2^m * J + R$ bits for compensating the interim address $i_0\ldots i_4$ in accordance with a column formed with the real value of the remainder R; Note: step 8 on page 2-111 of TIA/EIA/IS-2000.2-A-1 teaches that all addresses are retained including those in accordance with a column formed with the real value of the remainder R); and generating a read address by adding the interim address and the address compensation factor for the code symbol (see output of Figure 2.1.3.1.4.2.3-1 on page 2-111 of TIA/EIA/IS-2000.2-A-1; **Note: The Authoritative Dictionary of IEEE Standards Terms defined "add" as "to insert a record into an existing file" and Merriam-Webster's dictionary defines "add" as "to include as member of a group"**), and reading the code symbol written in the generated read address (see Turbo Interleaver in Figure 2.1.3.1.4.2.1-1 on page 2-109 of TIA/EIA/IS-2000.2-A-1); and decoding the code symbol read from the generated read address.

Note: the Interleaver/Deinterleaver taught in TIA/EIA/IS-2000.2-A-1 is taught for use in a CDMA2000 compliant communication system comprising turbo encoded data.

The Examiner asserts lines 8-11 of page 2-110 and Footnote 12 and page 2-111 in TIA/EIA/IS-2000.2-A-1 clearly teaches that the address generation is equivalent to writing turbo coded input bits to a $2^{n-1} * 2^5$ matrix at specific addresses specified by the input counter values to the Address calculator of Figure 2.1.3.1.4.2.3-1 on page 2-111 whereby the 5 LSBs $i_4\ldots i_0$ represent row addresses and the n MSBs represent $i_{n+4}\ldots i_5$

column addresses and whereby the output of the Address calculator of Figure 2.1.3.1.4.2.3-1 on page 2-111 represents the a read address form the $2^{n-1} * 2^5$ matrix. Figure 2.1.3.1.4.2.3-1 on page 2-111 in TIA/EIA/IS-2000.2-A-1 teaches that the row addresses $i_4 \ldots i_0$ are bit reversed to produce interim address $i_0 \ldots i_4$ and interim address $i_0 \ldots i_4$ is appended to address compensation factor $t_{n-1} \ldots t_0$ to generate a output read address. TIA/EIA/IS-2000.2-A-1 specifically teaches generating an interim address by bit reversal order (BRO) operation on an index of a code symbol as if the code symbols constitute a perfect 2m * J matrix (Bit reverse in Figure 2.1.3.1.4.2.3-1 on page 2-111 of TIA/EIA/IS-2000.2-A-1 is performed on the 5 LSBs independently of what R is and for all practical purposes R, that is, Bit reverse in Figure 2.1.3.1.4.2.3-1 and in step 6 on page 2-111 of TIA/EIA/IS-2000.2-A-1 is performed exactly the same way for any value R on each LSB address position $i_0 \ldots i_4$ as if the remainder R is 0 and as if the code symbols constitute a perfect $2^m * J$ matrix independent of the remainder R; $i_0 \ldots i_4$ in Figure 2.1.3.1.4.2.3-1 is an interim address; Note: Bit reverse is performed on row addresses $i_4 \ldots i_0$ independantly of the number of columns in the matrix and independently of whether there exits R remainder values)

The Examiner asserts that column addresses $i_{n+4} \ldots i_5$ correspond to columns of the $N_{turbo} = 2^m * J + R = 2^5 2^{n-1} + R$ bits in the $2^5 x 2^n$ element matrix of TIA/EIA/IS-2000.2-A-1. Figure 2.1.3.1.4.2.3-1 on page 2-111 in TIA/EIA/IS-2000.2-A-1 teaches that that column addresses $i_{n+4} \ldots i_5$ corresponding to all columns in the $2^5 x 2^n$ element matrix including the number of R code symbols written to the last column. Clearly TIA/EIA/IS-2000.2-A-1 teaches a step for generating an address compensation factor $t_{n-1} \ldots t_0$ for compensating

the interim address $i_0 \ldots i_4$ based on the number of the R code symbols written in the last column J since the address compensation factor $t_{n-1} \ldots t_0$ is based on column addresses $i_{n+4} \ldots i_5$ corresponding to all columns in the $2^5 x 2^n$ element matrix including the number of R code symbols written to the last column.

However TIA/EIA/IS-2000.2-A-1 does not explicitly teach the specific use of a turbo decoder for a CDMA2000 compliant communication system or decoding de-interleaved data.

Tiedemann, in an analogous art, teaches use of a turbo decoder for a CDMA2000 compliant communication system or decoding de-interleaved data (Figure 2 in Tiedemann).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TIA/EIA/IS-2000.2-A-1 with the teachings of Tiedemann by including use of a turbo decoder for a CDMA2000 compliant communication system or decoding de-interleaved data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a turbo decoder for a CDMA2000 compliant communication system or decoding de-interleaved data would have provided a CDMA2000 compliant communication system.

35 U.S.C. 103(a) rejection of claim 2.

Footnote 12 on page 2-111 of TIA/EIA/IS-2000.2-A-1 substantially teaches interleaving a sequence of length N_{turbo} by substantially mapping the N_{turbo} bits to a $2^5 x 2^n$ array

comprising 2^{n+5} positions in the array whereby $2^{n+4} \leq N_{turbo} \leq 2^{n+5}$; hence the sequence of length N_{turbo} is substantially mapped to $N_{turbo} = 2^{n+4} + R = 2^5 2^{n-1} + R$ positions in the $2^5 x 2^n$ array where R is the number of remainder bits exceeding the first 2^{n-1} columns and partially filling the remaining array.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is rejected on the ground of nonstatutory double patenting over claim 5 of U. S. Patent No. US 6668350 B1 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: claim 5 of U. S. Patent No. US 6668350 B1 clearly

suggests generating an interim address by bit reversal order, BRO, operation on an index of a code symbol (BRO(K/J) is an interim address of a bit reversal order, BRO, operation on an index of a code symbol); calculating an address compensation factor for compensating the interim address in consideration of the remainder (2^m(K mod J) is an address compensation factor for compensating the interim address in consideration of the remainder K mod J); and generating a read address by adding the interim address to the address compensation factor for the code symbol (BRO(K/J) + (2^m(K mod J) is a read address calculated by adding the interim address (BRO(K/J) to the address compensation factor (2^m(K mod J) for the code symbol).

In addition, claim 5 in U. S. Patent No. US 6668350 B1 explicitly recites, "calculating a third variable r corresponding to a remainder obtained by dividing a reading sequence K by the second variable J".

The Examiner would like to point out that the current rejections are based on the language in the claims and its relation to the cited art, not the "the scope of the present application" and its relation to the cited art. It is the Examiner's position that the current claim language that the Applicant uses to claim the Applicant's invention reads on the Prior Art. Specifically, claim 5 of U. S. Patent No. US 6668350 B1 is directed to generating read addresses from write addresses used to write input data to a 2^m * J matrix. Recited in the Applicant's claim 1 of the current application is a matrix that is a 2^m * J matrix with an additional column of R bits. This does not distinguish from claim 5 of U. S. Patent No. US 6668350 B1 since any 2^m * J matrix can be designated as 2^m * J' matrix with an additional column of R bits where J' = J-1 and R is equal to the number of

bits in the last column of the original 2^m * J matrix. Changing the way a matrix is described does not change the matrix. "The identical invention must be shown in as complete detail **as is contained in the ... claim**" [Emphasis added]. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, **but this is not an ipsissimis verbis test, i.e., identity of terminology is not required**. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Clearly BRO(K/J) is independent of the columns in the 2^m * J matrix (where the 2^m * J matrix can be designated as 2^m * J' matrix with an additional column of R bits where J' = J-1 and R is equal to the number of bits in the last column of the original 2^m * J matrix) including the last column since BRO(K/J) since K/J only depends on the number of columns K/J=2^m in the 2^m * J matrix. Furthermore, (2^m(K mod J) is based on every value in the original 2^m * J matrix including the last column of R bits (where the 2^m * J matrix can be designated as 2^m * J' matrix with an additional column of R bits where J' = J-1 and R is equal to the number of bits in the last column of the original 2^m * J matrix).

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott T. Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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